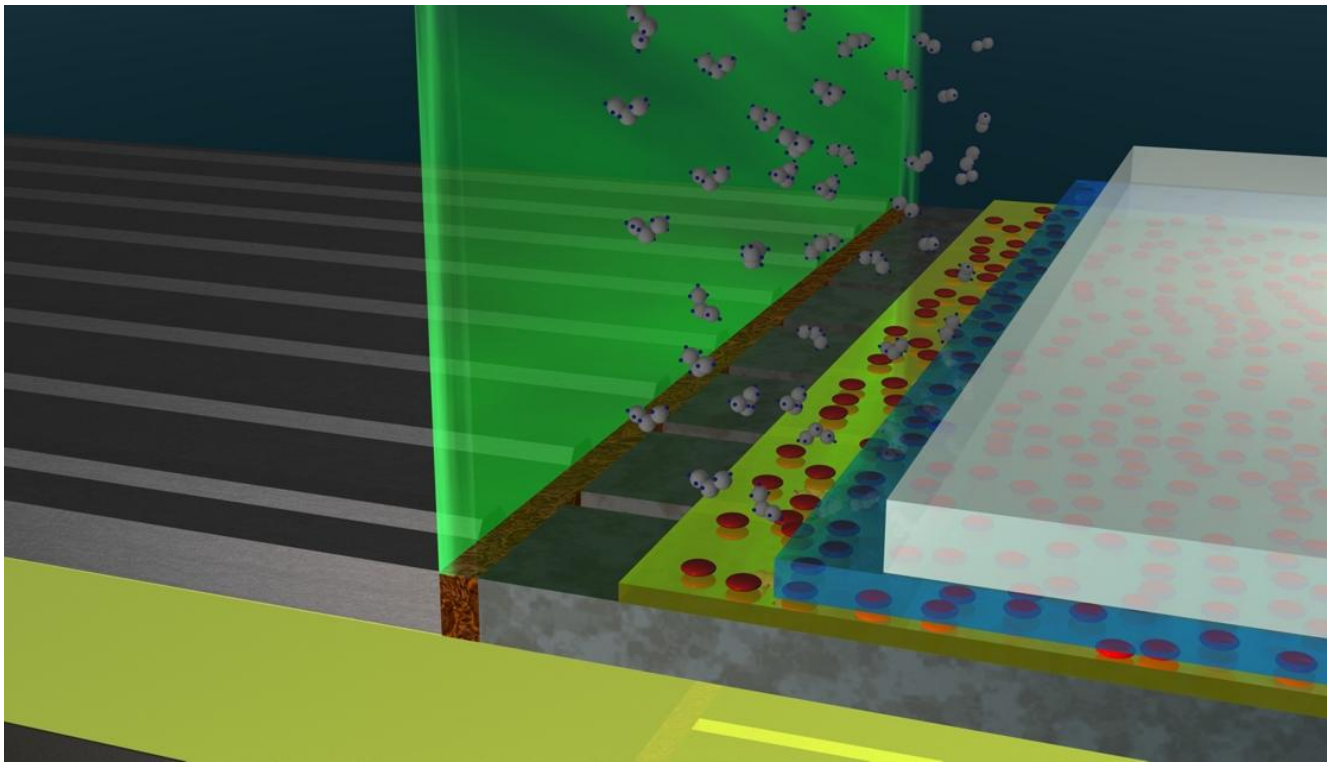
Device fabrication at CMOS back-compatible temperatures.



Shown illustration gives a schematical overview of the process steps used during the low-temperature fabrication of the non-volatile memory devices. Starting from the left side of the figure, the preformed amorphous silicon film on top of silicon oxide is shown. Then the silicon crystallization process (i.e. transformation from amorphous in to polycrystalline) is done using green-laser annealing. The scanning type of annealing in combination with special film morphology results in to the long single-grain regions almost without grain boundaries. Those high-quality regions could be used for further device manufacturing. Right part of the figure shows the formation of functional multilayer stack using various low-temperature deposition techniques (e.g. ICPECVD for SiO_2, LPCVD for silicon nanodots, ALD for Al_2O_3, etc.). Especially interesting is the deposition of the silicon nanodots, which is highlighted in the picture.

This static artwork provides already a lot of information about the processes. However, if it could be possible to enliven it, and to show all steps, starting with a-Si deposition and finishing with electrical measurements of the memory cell, it becomes fascinating self-sufficient story about entire low-temp device processing.